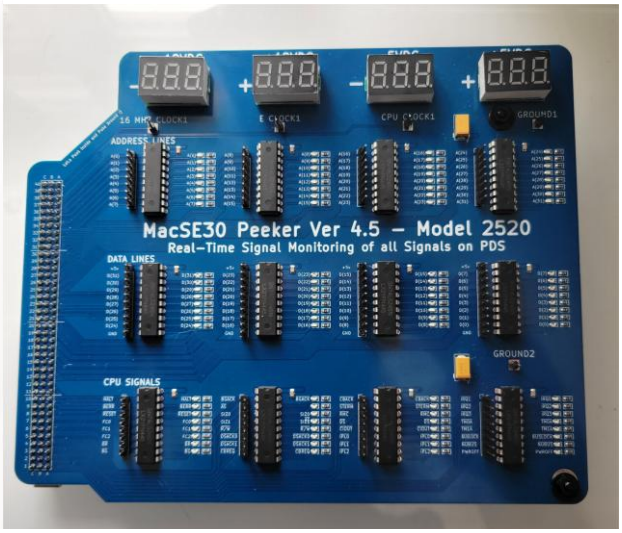
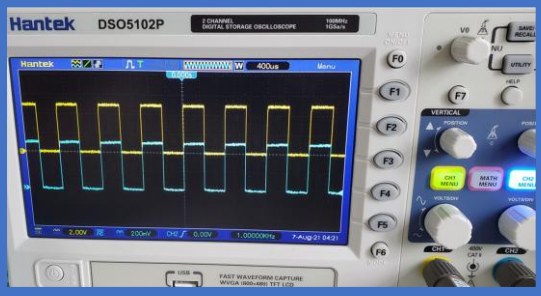
Rudy’s Retro Intelligence





Apple Macintosh SE/30 Peeker

Version 4.5 Created in March 2025

Created by Rudy's Retro Intel

The purpose of the Mac SE/30 Peeker is to help identify issues, provide real time monitoring of important signals, and assist in the repair of an Apple Macintosh SE/30 computer.

For the latest version of this document and other diagnostic manuals, use the links below.
https://github.com/RudyRetroIntel/Vintage-Computer-Diagnostics also you can find my videos here:
https://www.youtube.com/@RudysRetroIntel

Features

- Plugs directly into the Processor-Direct Slot (PDS) for plug and play.
- Real time viewing of power voltages for +5VDC, -5VDC, +12DC, and -12VDC.
- Ability to monitor all voltages for power fluctuations in real time.
- Real time viewing of all address line signals – A0 to A31.
- Real time viewing of all data line signals – D0 to D31.
- Real time viewing of support signals. See page 4 for list of all support signals.
- Ability to access all signals via oscilloscope with access points next to each SMD LED and label
- Direct access to CPU clock and 16Mhz clock.
- Board does not interfere with access to other components on the motherboard

Please note that this board is only for the SE/30 and is not intended to use with other computers unless they are compatible with cards from the SE/30.

Contributors

Jason aka @GutBomb. https://gutbomb.net/
Jason volunteered to perform testing, validation and help diagnose initial issues with the prototypes. His inputs, testing, troubleshooting and design suggestions helped make this project a success.

Steve aka @Mac84. https://www.youtube.com/@Mac84
Volunteered to provide additional feedback and testing.

***** This document is based on the work I and others have performed on their Macintosh SE/30 computer and is provided "as is". I\we do not take any responsibility for errors and\or damages that may occur when repairing your computer and\or using this product. This information is provided freely to all SE/30 computer owners. Please ensure you know how to perform electronics\electrical work. If not, please contact someone who has these skills before starting. *****

Index

MAC SE/30 Peeker Signal Information

Below is the legend for each of the signals shown and are real time monitored.

Name	Description	Name	Description	Name	Description
/IRQ1	Interrupt Request 1	/BG	BUS Grant	/RESET	System Reset
/IRQ2	Interrupt Request 2	/BGACK	BUS Grant Ack	/BERR	BUS Error
/IRQ3	Interrupt Request 3	/BR	BUS Request	/HALT	Halt of 68030
/IPL0	IPL0	R/W	Read Write	16M	16 MHz Clock
/IPL1	IPL1	/AS	Address Strobe	CPUCLOCK	CPU Clock
/IPL2	IPL2	/RMC	Read Modify Cycle	/BUSLOCK	BUS Clock
SIZ0	Transfer Size bit 0	/CIOUT	Cache Inhibit Out	GND	Ground
SIZ1	Transfer Size bit 1	/CBACK	Cache Burst Ack	PWROFF	Power Off
D0 - D31	Data Lines	/CBREQ	Cache Burst Req		
A0 - A31	Address Lines	FC0	Function Code 0		
/DSACK0	Data Ack 0	FC1	Function Code 1		
/DSACK1	Data Ack 1	FC2	Function Code 2		
/DS	Data Strobe	/STERM	Sync. Cycle Termination		

The "/" indicates signal is Active LOW.

See Page 21 for complete details of signals listed above

Realtime voltage displays show the following voltages:

+12 VDC
+5 VDC
-5 VDC
-12 VDC

Testing has shown that the meters are only off by **0.01** to **0.10** volts. This is good enough for testing, validation of power, and monitoring for power fluctuations.

The Motorola 68030 CPU signals are read in and monitored via the 120 pins on the PDS (Processor-Direct Slot). Only data available via the PDS is displayed. Additional signal may be viewed\monitored directly from the motherboard.

Assembly of the Mac SE/30 Peeker Board

The board is provided as a kit which means that some components will need to be soldered to the board. The bulk of the soldering is already complete as there are many “Surface Mounted Devices” (SMD) LEDs. To complete the project, you will need to solder the following:

- Voltage meters
- PDS connector

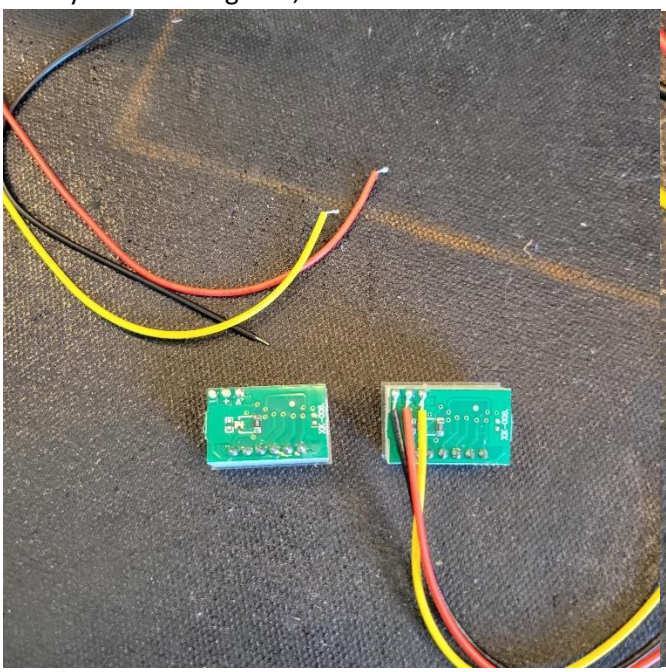
When assembling, it is recommended that you follow the following steps. If not, you could install components incorrectly.

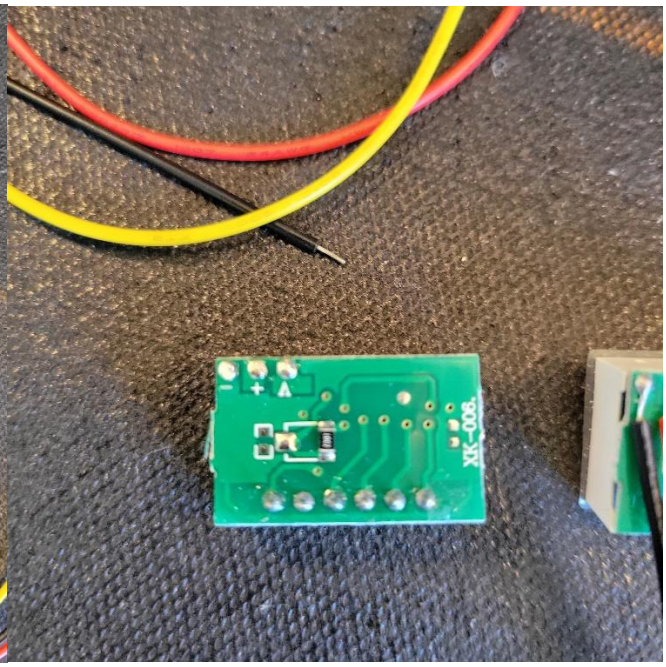
1. Installation of Voltage Meters
2. Installation of PDS Connections

Step 1. Installation of Voltage Meters

To install the voltage meters, you need to perform the following steps for each meter for proper installation.

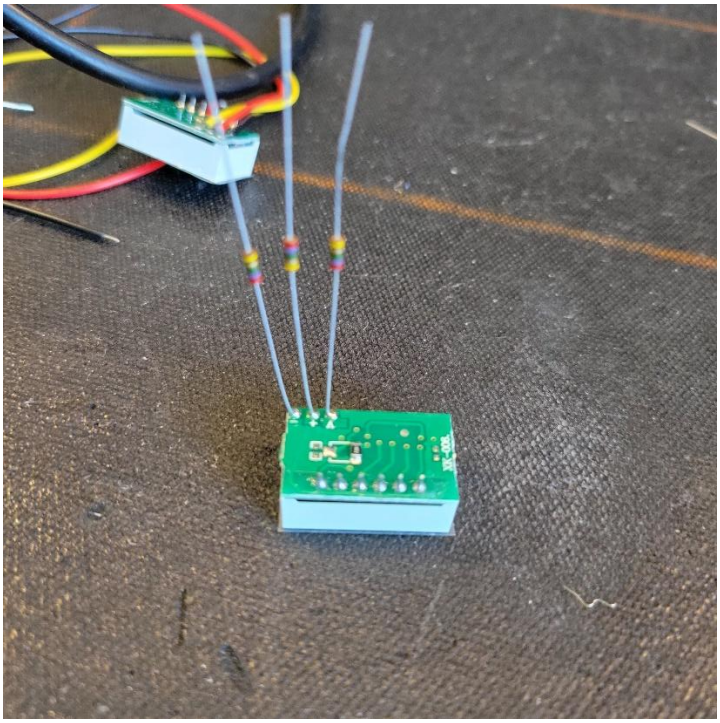
a. With your soldering iron, remove the 3 wires attached.



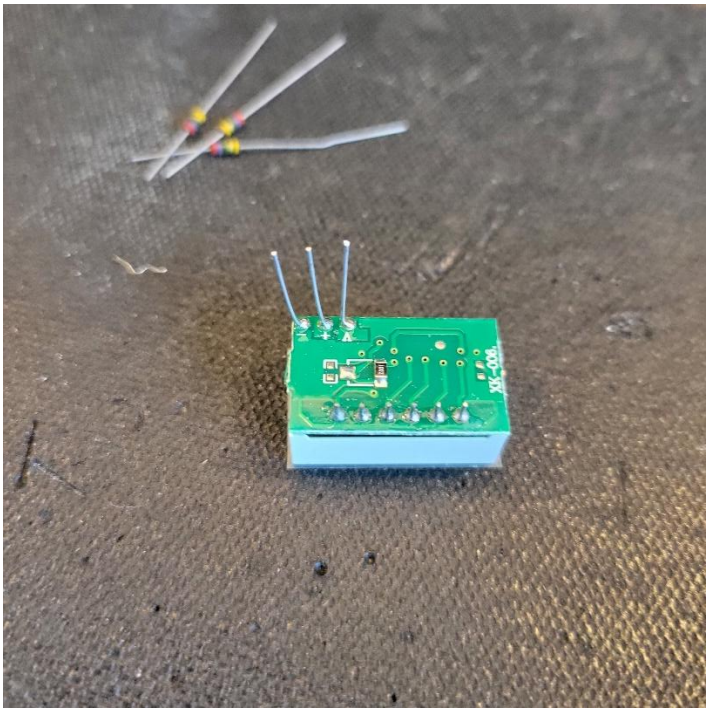


b. Cut the section off that has the mounts for screws. This is not needed as the solder will hold the meter into place.

c. Collect several resistors, values don't matter as you will only be using the legs. You can also use other metal wires for this step. Ensure the legs will fit through the holes on the board before continuing.

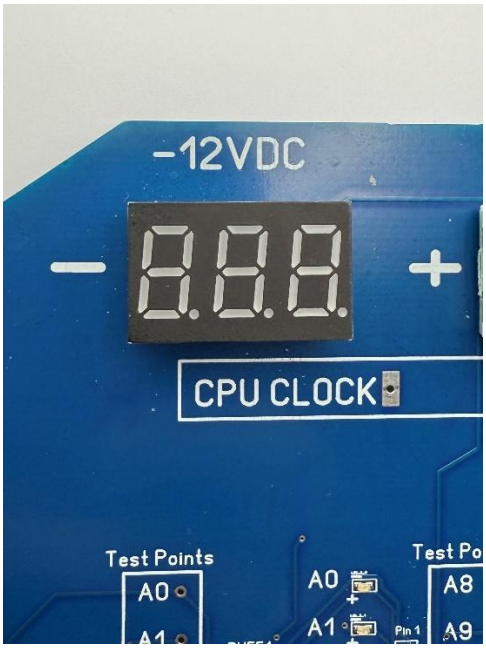


d. Solder in place the 3 resistors so that the leg just barely extends pass the board.



e. Leave approx. ¾ of an inch or 1cm and cut off the rest of the resisters. Use the remaining leads for the other meters.

f. Install the meter so that the 3 legs poke through the board and the rear pins of the meter are placed in corresponding holes.



g. Solder the 3 legs then place solder on the additional holes. These pins may not protrude the back of the board, but just place solder to fill each hole as it this help hold the meter to the board.

h. Repeat for each of the 4 voltage meters.

Step 2. Installation of Stand Offs

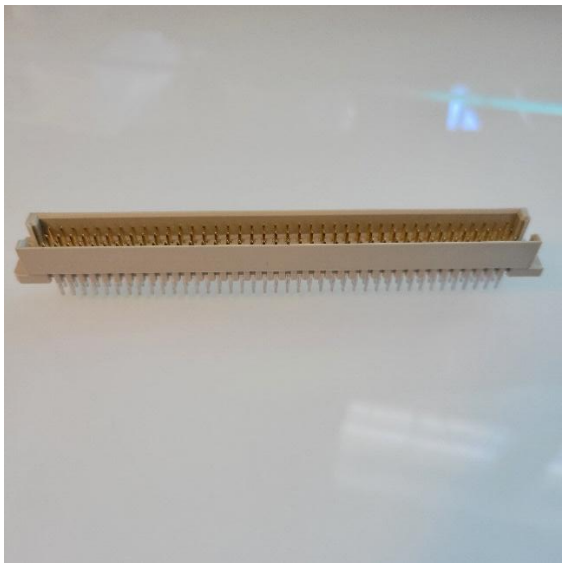
There are 2 holes on the board which allow you install offs. You can use nylon\plastic stand offs at are 20mm in length. *Stand offs are not included in this kit however you can find them on Amazon.*

NOTE: This step is recommended to do before moving to step 4 to help with PIN alignment of the PDS connector. It also helps support the Peeker board once installed on the Mac SE30.

Step 3. Installation of PDS Connections

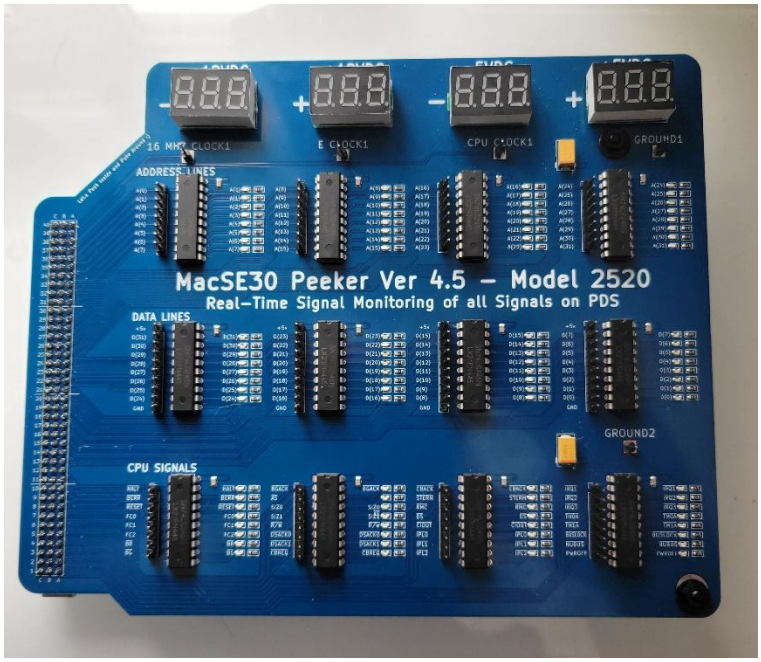
This is the final step. The kit comes with male connector for the PDS.

Male PDS Connector



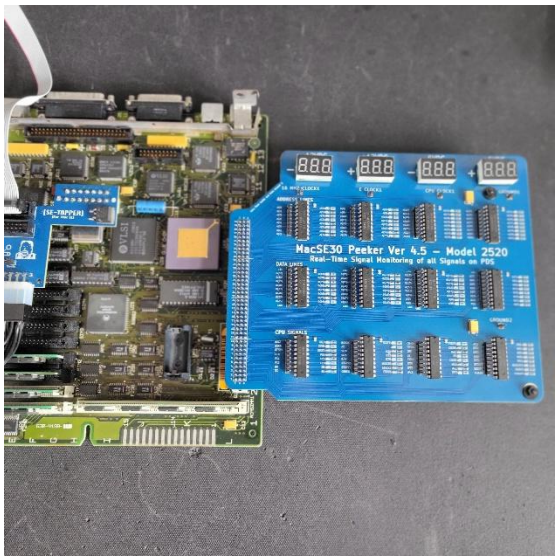
Using the PDS slot of the Macintosh SE/30, insert the connector into the PDS slot of the SE/30. This will leave the pins facing upwards. Place the Peeker board on top and solder the pins to the board. I would recommend just soldering a few then pull it off and finish the rest. This way, you don't over heat the PDS female connector on your SE30. *The reason for installing the PDS connector this way, is to ensure you don't solder it on backwards or on the wrong side.*

When installing and soldering the PDS connectors, ensuring that the voltage meters and LEDs are facing upwards as that is the top of the board. If not, the board will not work. When completed your board should look like the picture below.

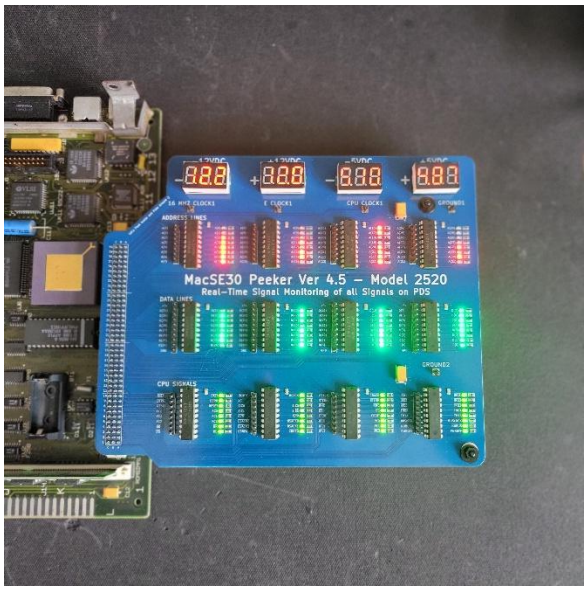


Installation and Usages

To use the board, place the Macintosh SE/30 on your bench, ensuring the slot is located to your right. Align the Peeker board on top of the slot and press down, ensuring all the pins are inserted into the PDS. If misaligned damage may occur to either board. The Peeker board should be hanging off the side of the SE/30 motherboard.



Power up the SE/30 and you should see LEDs flashing and the meters showing voltages, like the image below.



If nothing is working, check the following:

A. Peeker board is inserted correctly.
B. Power supply is working.
C. Ensure the AC plug for the power supply is connected and working.

Measuring Signals with Oscilloscope

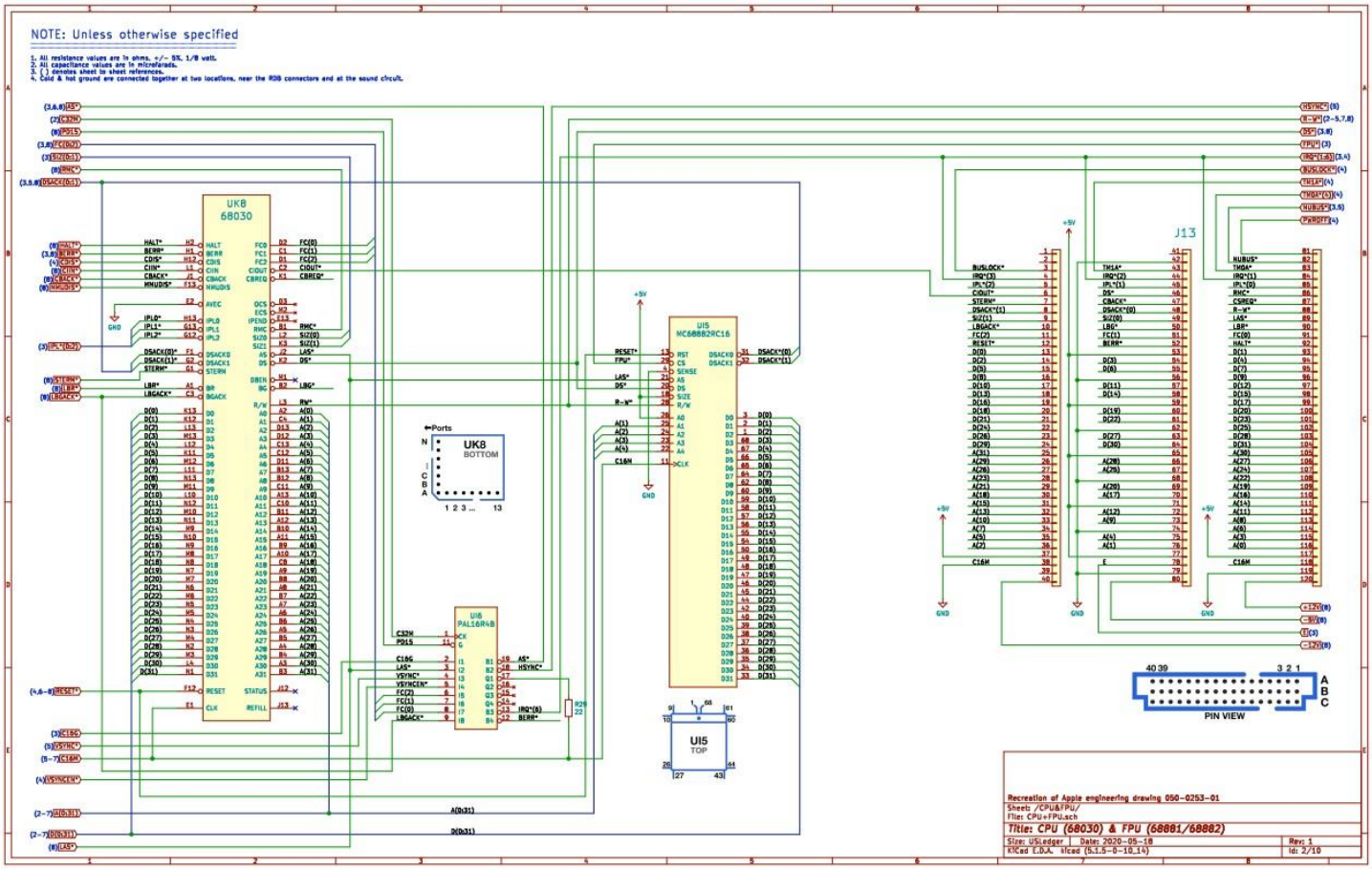
Each LED has a small connection point where the oscilloscope can be place. With power on, place the oscilloscope probe on this point to get measurement. Adjust oscilloscope so that measurements can be shown\read.

Apple Macintosh SE/30 Schematics

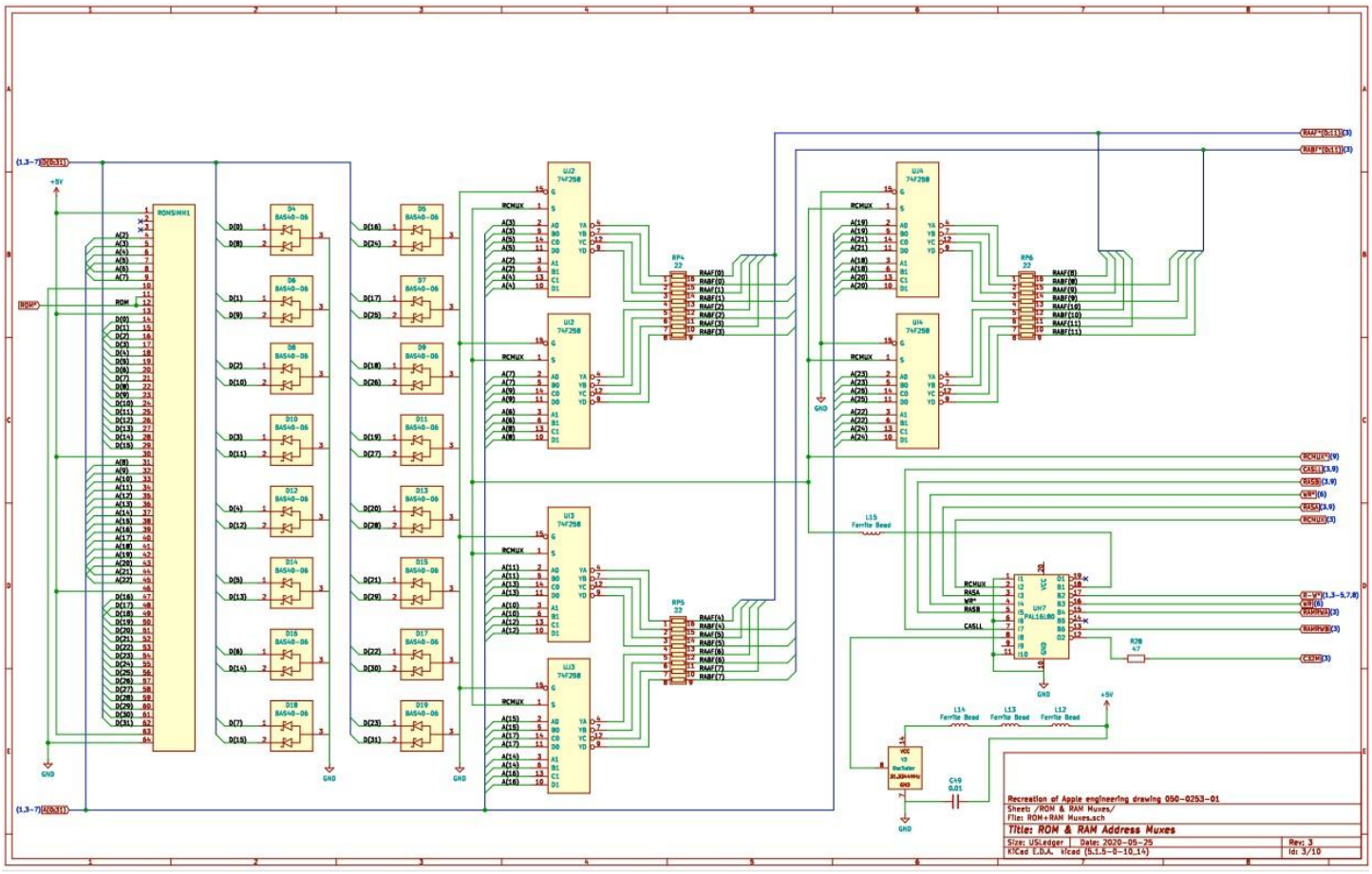
You can find the schematics here:
https://github.com/mishimasensei/macse30mlb/blob/master/hardware/pcb/mlb/output/Macintosh%20SE%3A30%20Schematic%20Redraw%20of%20050-0253-01%20JUL-26-2022.pdf

Credit to elemenoh for remaking these schematics.

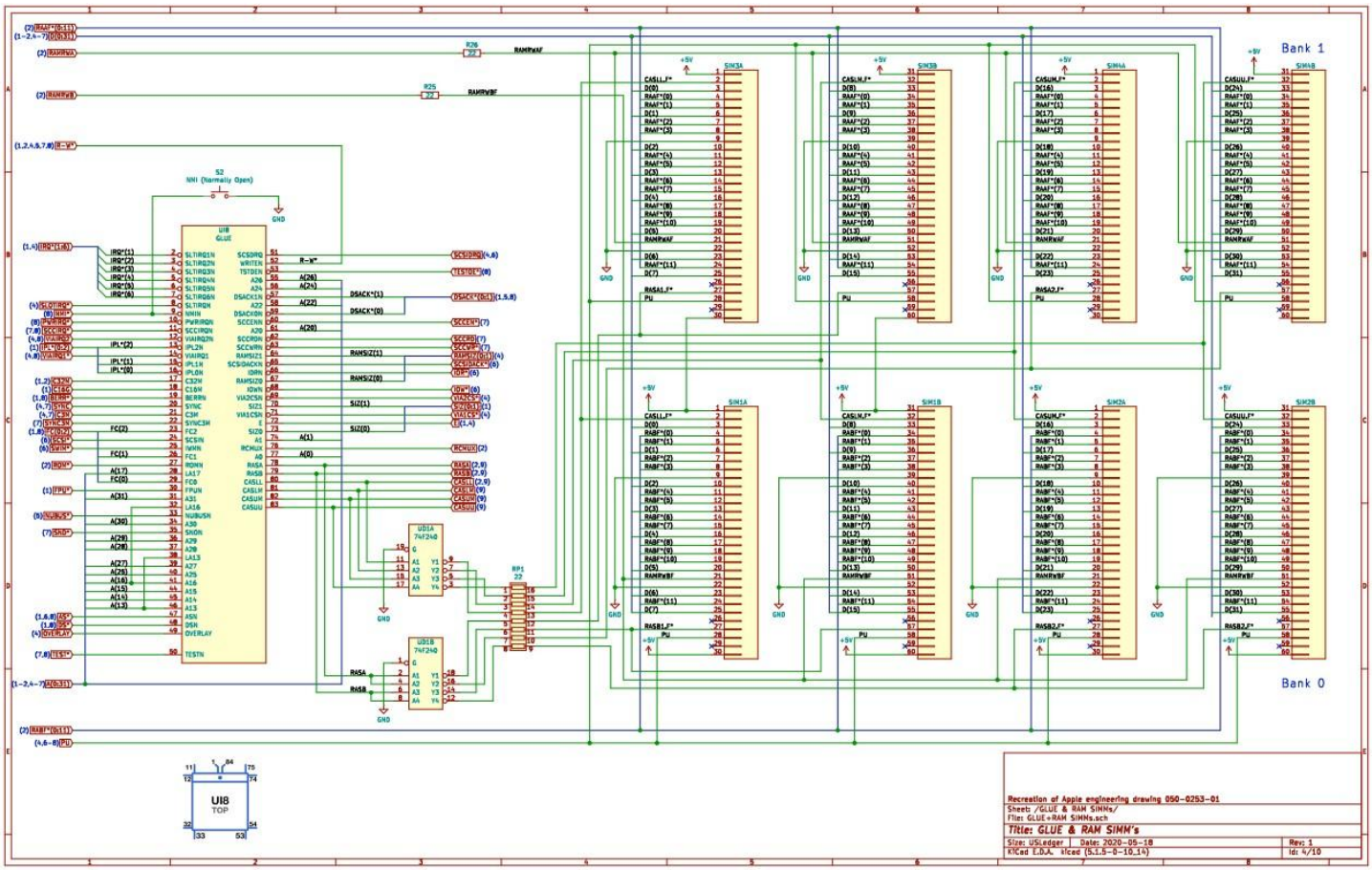
CPU and FPU



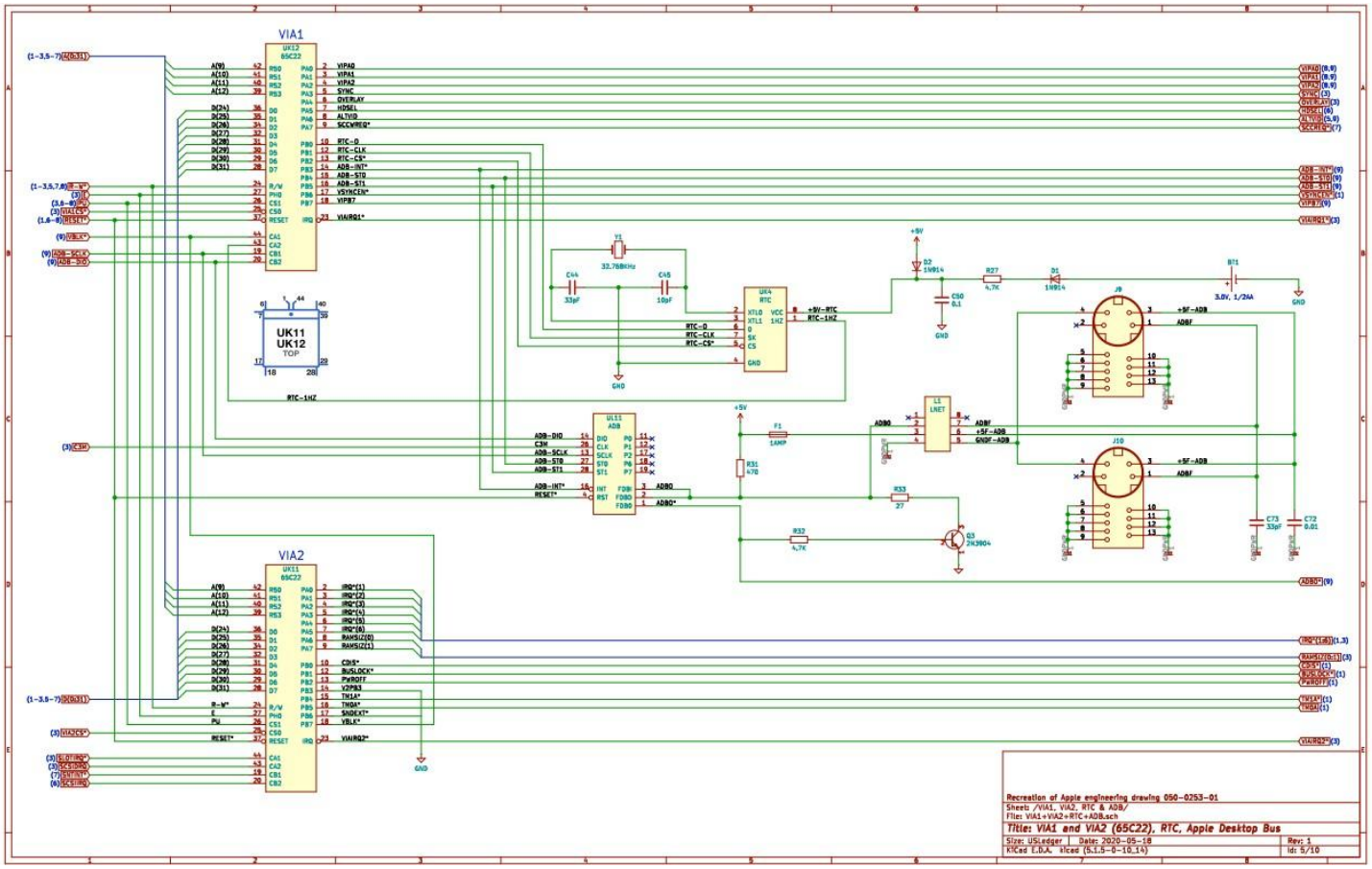
ROM and RAM Address



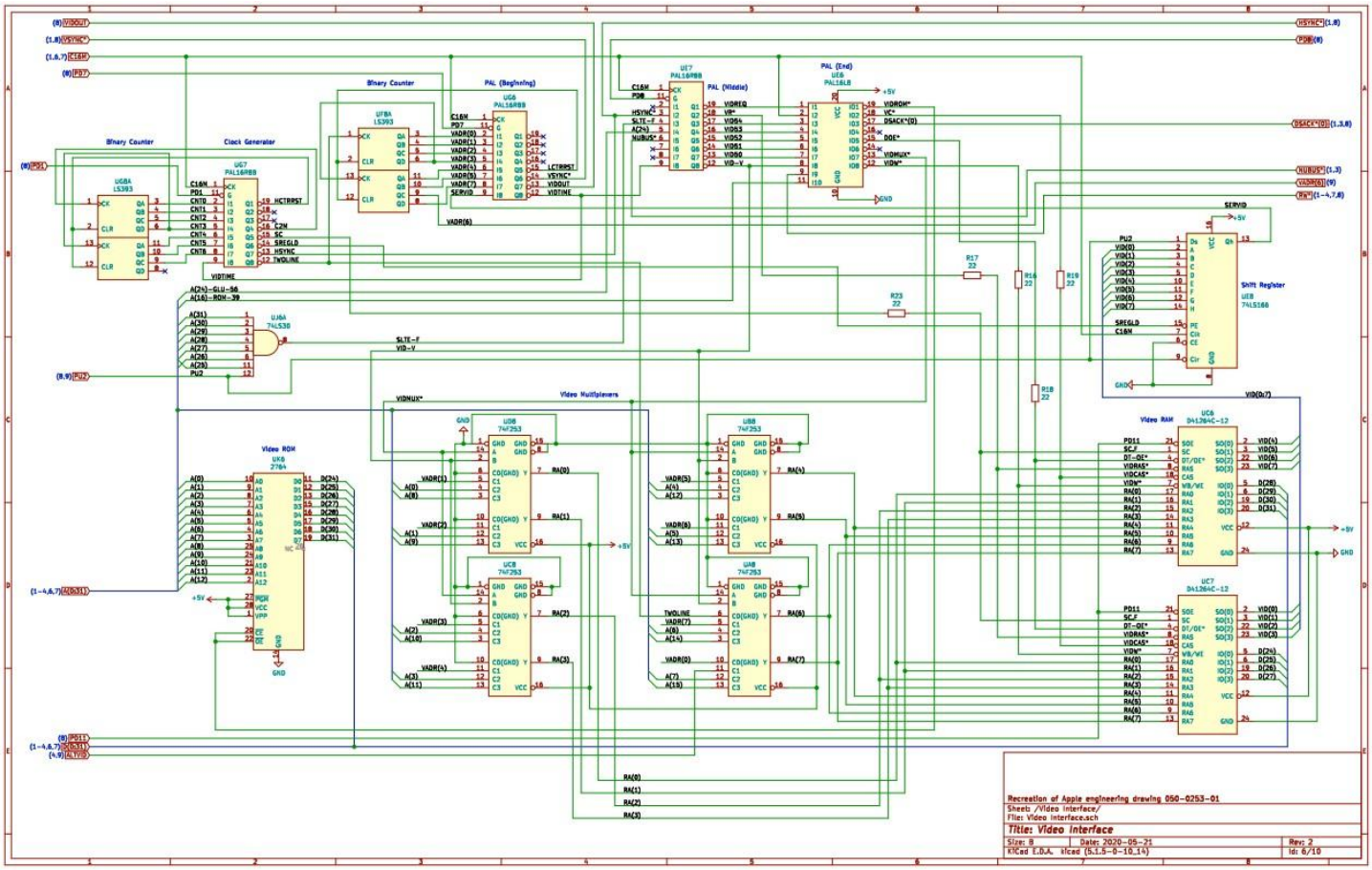
Glue Chip RAM SIMMs



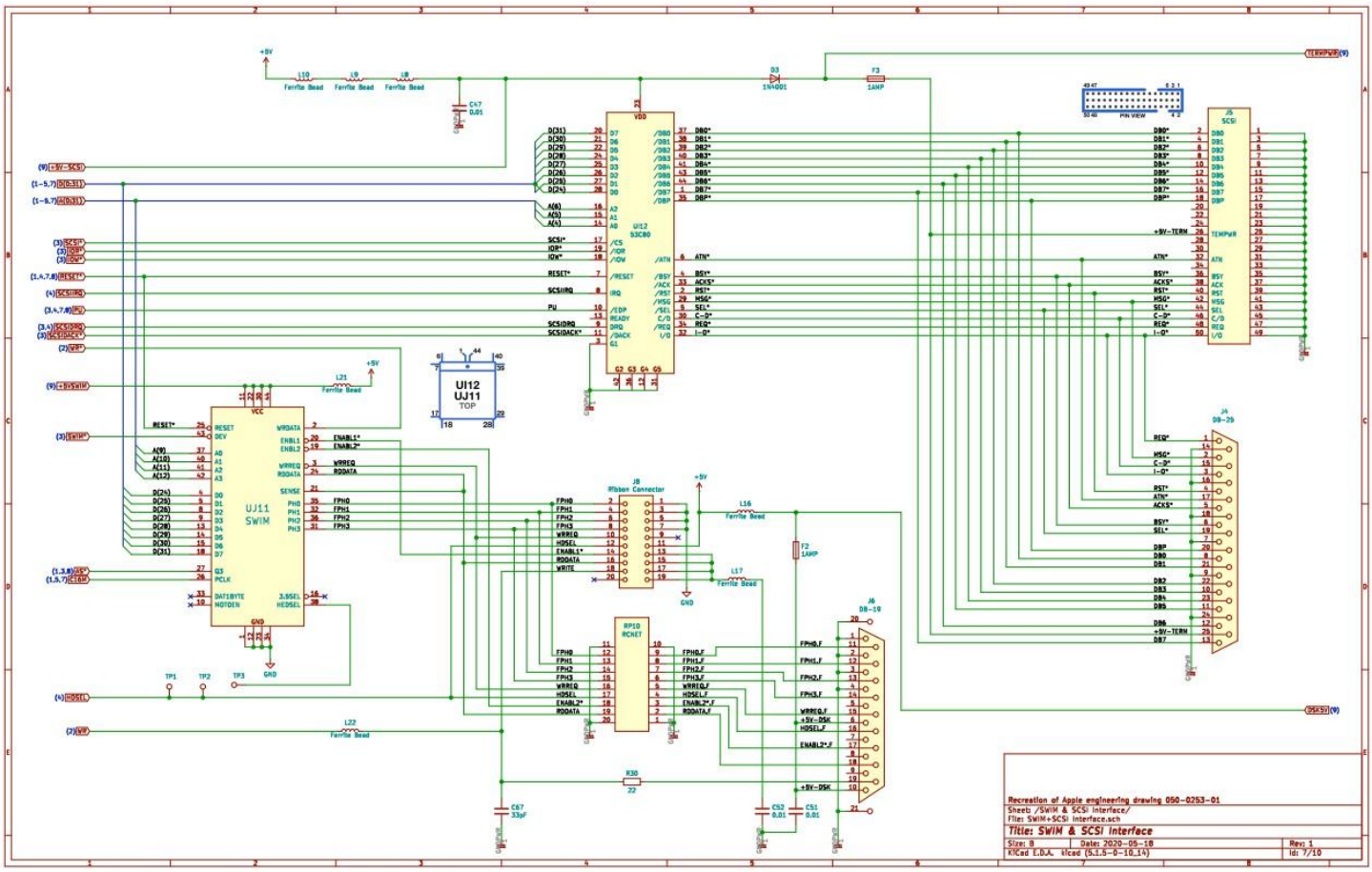
VIA1 and VIA2 (65C22, RTC, Apple Desktop BUS



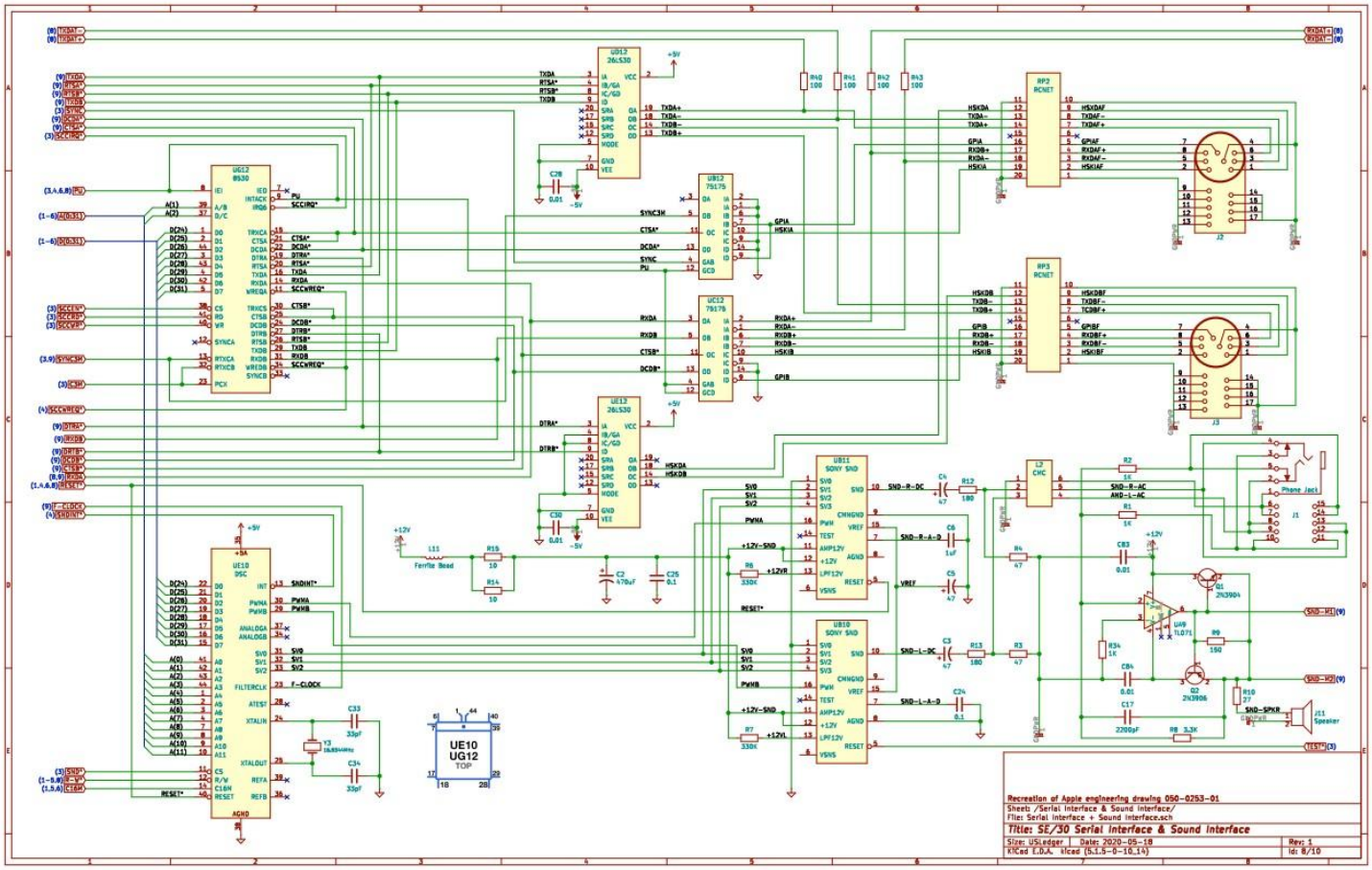
Video Interface



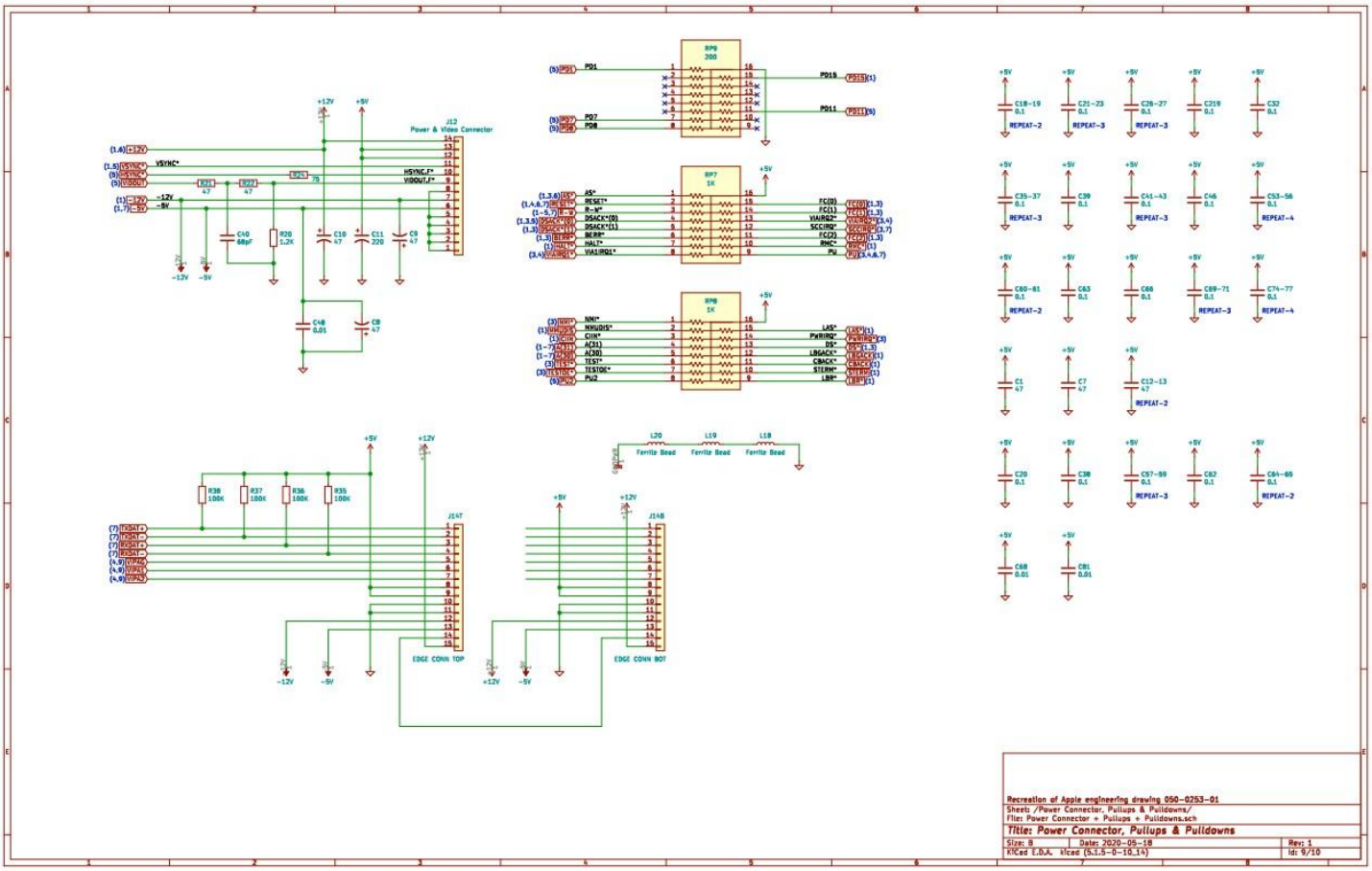
SWIM and SCSI Interface



Serial Interface and Sound Interface



Power Connector, Pull Ups and Pull Downs



Data Lines Matrix

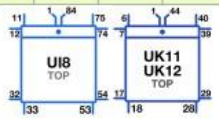
Macintosh SE/30 MLB Data Line Pin Matrix

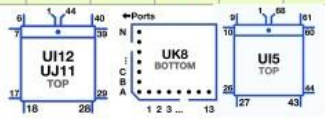
Address	ROM	D4 Diode	D5 Diode	D6 Diode	D7 Diode	D8 Diode	D9 Diode	D10 Diode	D11 Diode	D12 Diode	D13 Diode	D14 Diode	D15 Diode	D16 Diode	D17 Diode	D18 Diode	D19 Diode	S1A RAM	S1B RAM	S2A RAM	S2B RAM	S3A RAM	S3B RAM	S4A RAM	S4B RAM	UK12 VIA1	UK11 VIA2	UK6 VROM	UC6 VRAM	UC7 VRAM	UJ11 SWIM	UI12 SCSI	UG12 Serial	UE10 DSC	UK8 CPU	UI5 FPU	J13 PDS
D(0)	14	1																3				3													K13	3	13
D(1)	15			1														6				6													K12	2	93
D(2)	16					1												10				10													L13	1	14
D(3)	17							1										13				13													M13	68	54
D(4)	18									1								16				16													L12	67	94
D(5)	19											1						20				20													K11	66	15
D(6)	20													1				23				23													M12	65	55
D(7)	21															1		25				25													L11	64	95
D(8)	22	2																	3				3												N13	62	16
D(9)	23			2															6				6												M11	60	96
D(10)	24					2													10				10												L10	59	17
D(11)	25							2											13				13												N12	58	57
D(12)	26									2									16				16												M10	57	97
D(13)	27											2							20				20												N11	56	18
D(14)	28													2					23				23												M9	55	58
D(15)	29															2			25				25												N10	54	98
D(16)	47		1																	3				3											N9	50	19
D(17)	48				1															6				6											M8	49	99
D(18)	49						1													10				10											N8	48	20
D(19)	50								1											13				13											N7	47	60
D(20)	51										1									16				16											M7	46	100
D(21)	52												1							20				20											N6	45	21
D(22)	53														1					23				23											M6	44	61
D(23)	54																1			25				25											N5	42	101
D(24)	55		2																		3				3	36	36	11		5	4	28	1	22	M5	40	22
D(25)	56				2																6				6	35	35	12		6	5	27	2	21	N4	39	102
D(26)	57						2														10				10	34	34	13		19	8	26	44	20	N3	38	23
D(27)	58								2												13				13	32	32	15		20	9	25	3	19	M4	37	63
D(28)	59										2										16				16	31	31	16	5		13	24	43	18	N2	36	103
D(29)	60												2								20				20	30	30	17	6		14	22	4	17	M3	35	24
D(30)	61														2						23				23	29	29	18	19		15	21	42	16	L4	34	64
D(31)	62																2				25				25	28	28	19	20		18	20	5	15	N1	33	104

Address Lines Matrix

Macintosh SE/30 MLB Address Line Pin Matrix

Address	ROM	UJ2 RAM Mux	UI2 RAM Mux	UI3 RAM Mux	UJ3 RAM Mux	UJ4 RAM Mux	UI4 RAM Mux	UI8 GLUE	UK12 VIA1	UK11 VIA2	UK6 Vid ROM	UA8 Video Mux	UB8 Video Mux	UC8 Video Mux	UD8 Video Mux	UJ11 SWIM	UG12 Serial	UE10 Sound	UK8 CPU	UI5 FPU	J13 PDS Slot
A(0)								77			10				4			41	A2		116
A(1)								74			9				12		39	42	C4	25	76
A(2)	4	3,6									8			4			37	43	D13	24	36
A(3)	5	2,5									7			12				44	D12	23	115
A(4)	6	10,13									6		4					1	C13	22	75
A(5)	7	11,14									5		12					2	C12		35
A(6)	8		3,6								4	4						3	D11		114
A(7)	9		2,5								3	12						4	B13		34
A(8)	31		10,13								25				3			7	B12		113
A(9)	32		11,14						42	42	24				13	37		8	C11		73
A(10)	33			3,6					41	41	21			3		40		9	A13		33
A(11)	34			2,5					40	40	23			13		41		10	C10		112
A(12)	35			10,13					39	39	2		3			42			B11		72
A(13)	36			11,14				46					13						A12		32
A(14)	37				3,6			45											B10		111
A(15)	38				2,5			44											A11		31
A(16)	39				10,13			41											B9		110
A(17)	40				11,14			28											A10		70
A(18)	41					3,6													C8		30
A(19)	42					2,5													A9		109
A(20)	43					10,13		61											B8		69
A(21)	44					11,14													A8		29
A(22)	45						3,6	58											B7		108
A(23)							2,5												A7		28
A(24)							10,13	56											A6		107
A(25)							11,14	40											B6		67
A(26)								55											A5		27
A(27)								39											B5		106
A(28)								37											A4		66
A(29)								36											B4		26
A(30)								34											A3		105
A(31)								31											B3		25





Signal Details:

Name	Description	Name	Description	Name	Description
/IRQ1	Interrupt Request 1	/BG	BUS Grant	/RESET	System Reset
/IRQ2	Interrupt Request 2	/BGACK	BUS Grant Ack	/BERR	BUS Error
/IRQ3	Interrupt Request 3	/BR	BUS Request	/HALT	Halt of 68030
/IPL0	IPL0	R/W	Read Write	16M	16 MHz Clock
/IPL1	IPL1	/AS	Address Strobe	CPUCLOCK	CPU Clock
/IPL2	IPL2	/RMC	Read Modify Cycle	/BUSLOCK	BUS Clock
SIZ0	Transfer Size bit 0	/CIOUT	Cache Inhibit Out	GND	Ground
SIZ1	Transfer Size bit 1	/CBACK	Cache Burst Ack	PWROFF	Power Off
D0 - D31	Data Lines	/CBREQ	Cache Burst Req		
A0 - A31	Address Lines	FC0	Function Code 0		
/DSACK0	Data Ack 0	FC1	Function Code 1		
/DSACK1	Data Ack 1	FC2	Function Code 2		
/DS	Data Strobe	/STERM	Sync. Cycle Termination		

The "/" indicates signal is Active LOW.

Interrupt Request (1-3)

An interrupt request (IRQ) is a signal sent to the CPU by hardware devices or software indicating that they need immediate attention. When the CPU receives an IRQ, it temporarily halts its current tasks, saves its state, and executes an interrupt service routine (ISR) to address the request.

IRQs are used to manage various hardware components and ensure efficient communication between them. For example, the SE/30 has multiple IRQ lines, such as IRQ1, IRQ2, and IRQ3, which are used by different peripherals and system components.

IPLO (0-2)

This signal is used for interrupt handling (Interrupt Priority Level). It's part of the system's interrupt logic, helping manage and prioritize various interrupt requests from different hardware components.

SIZO-SIZ1

This signal is used to indicate the size of the data transfer occurring between the CPU and peripheral devices.

DSACK (0 -1)

The Data Acknowledge (DSACK) signal is used to acknowledge data transfers between the CPU and peripheral devices via the Processor-Direct Slot (PDS). It ensures that data has been successfully transferred and received, helping maintain efficient communication within the system.

DS

The Data Strobe (DS) signal is used in computer architecture for asynchronous data transfer. It's a control line that helps synchronize data transfers between devices. Here's a brief overview:

- Purpose: The Data Strobe signal ensures that data is transferred accurately and at the right time between the source (e.g., CPU) and the destination (e.g., memory or I/O device).
- Operation: When the source places data on the data bus, it activates the Data Strobe signal to indicate that valid data is available. The destination unit reads the data when it detects the Data Strobe signal.
- Handshaking: The Data Strobe method is a form of handshaking, where the source and destination coordinate the timing of data transfers to ensure reliable communication.

BG

The Bus Grant signal is used in computer architecture to indicate that the CPU (or bus arbiter) has granted access to the system bus to a device controller. This allows the device to either start an interrupt or perform Direct Memory Access (DMA) transfers to main memory. Essentially, it's a way for the CPU to manage and coordinate access to the system bus, ensuring smooth communication and data flow between the CPU and peripheral devices.

BGACK

Bus Grant Acknowledge is used in computer architecture to indicate that a device has acknowledged the bus grant signal from the CPU, allowing it to proceed with data transfer or other bus-related activities.

BR

The Bus Request signal is used by a device to request access to the system bus. When a device needs to perform data transfer or other bus-related activities, it sends a Bus Request signal to the CPU or bus arbiter, indicating that it needs access to the bus.

Read Write

Read and Write signals are crucial for data transfer between the CPU and memory or peripheral devices. Here is a brief overview:

- Read Signal: Informs a memory or I/O device that the CPU wants to read data from it. The device places the requested data on the data bus for the CPU to access.
- Write Signal: Indicates that the CPU wants to write data to a memory or I/O device. The device then reads the data from the data bus and stores it in the appropriate location.

AS

The AS signal stands for Address Strobe. In computer systems, it plays a crucial role in the communication between the CPU and memory or I/O devices:

- Purpose: The Address Strobe signal indicates that a valid address is present on the address bus. This signal helps synchronize the transfer of data between the CPU and other components.
- Operation: When the CPU places a valid address on the address bus, it asserts the Address Strobe signal. This informs the memory or I/O device that the address is ready and valid for a read or write operation.

The Address Strobe signal ensures that data is transferred accurately and efficiently within the system.

RMC

A Read-Modify-Write (RMW) cycle is a type of processor bus cycle used in computer systems to perform atomic operations. Here's a brief overview:

- Purpose: The RMW cycle is used to read a value from a memory location, modify it, and then write the modified value back to the same location. This ensures that the read and write operations are performed as a single, indivisible unit, which is crucial in multiprocessor systems to prevent race conditions.
- Operation: The processor initiates the RMW cycle by placing the address of the memory location on the address bus. Once the address is stable, the processor asserts the address strobe signal. The processor then reads the data from the memory location, modifies it, and writes the modified data back to the same location.

This cycle is often used in locking mechanisms to ensure data consistency and integrity.

CIOUT

The Cache Inhibit Out signal is used in computer systems to control the caching mechanism. When this signal is active, it prevents the cache from storing or retrieving data, effectively bypassing the cache. This can be useful in situations where direct access to memory is needed without the latency introduced by cache operations.

CBACK

The Cache Burst Acknowledge signal is used in computer systems to acknowledge the completion of a burst data transfer. When a burst of data is transferred between the CPU and memory or another device, the CBACK signal indicates that the burst has been successfully received and processed.

CBREQ

The Cache Burst Request signal is used in computer systems to initiate a burst data transfer between the CPU and memory or another device. When a burst of data needs to be transferred, the Cache Burst Request signal is sent to start the process, allowing for efficient and rapid data movement.

FC (0-2)

Function Code is used in various computing contexts to indicate a specific operation or status. Function Code is used for field-encoding operations. This involves encoding data according to specified rules before it is stored or processed further.

STERM

The Synchronous Termination signal is a bus handshake signal. This signal indicates that the address port size is 32 bit and the data is to be latched on the next falling clock edge for a read cycle.

REST

This is a bidirectional signal use to initiate a system rest.

BERR

A Bus Error (SIGBUS) is a hardware fault that occurs when a process tries to access memory that the CPU cannot physically address. This usually happens due to one of the following reasons:

1. Non-existent Address: The CPU is instructed to read or write to a physical memory address that doesn't exist.
2. Unaligned Access: The CPU tries to access data at an address that isn't properly aligned for the data type being accessed.

When a bus error occurs, the operating system typically sends a SIGBUS signal to the process, which can cause the process to terminate.

HALT

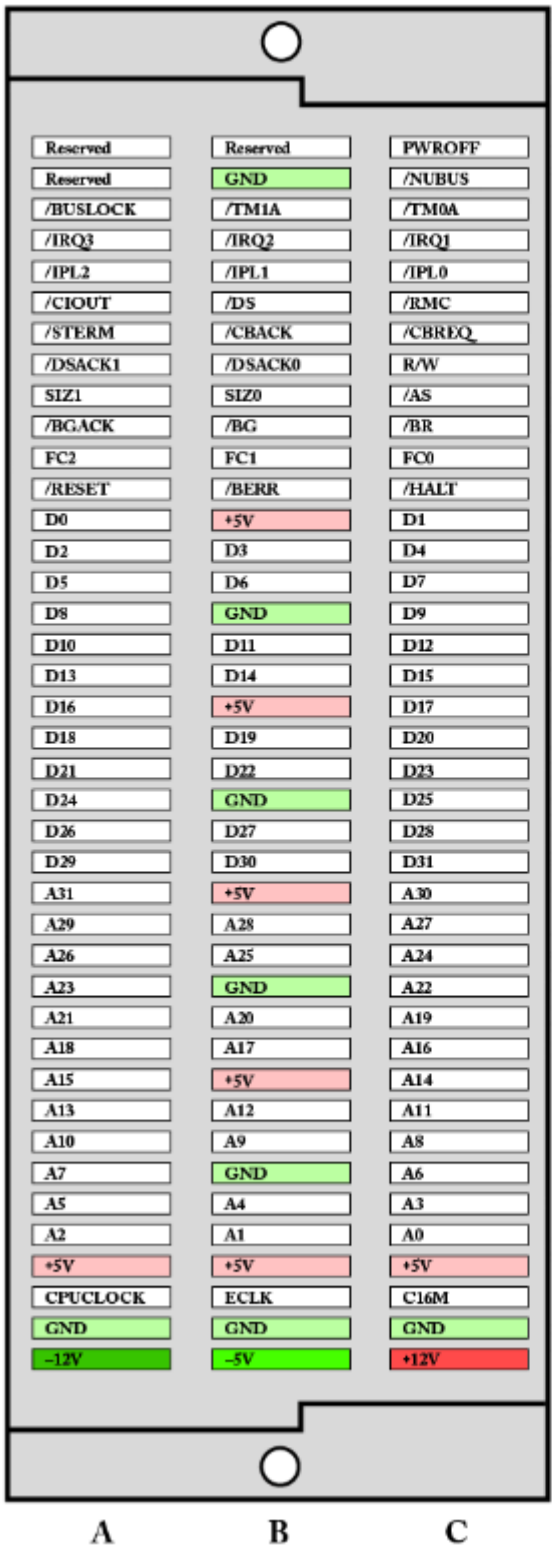
The HALT signal is used to indicate that a process or operation stop immediately. It's a way to halt the execution of a task, usually in response to an error or specific condition that requires immediate attention.

BUSLOCK

The BUSLOCK signal is used to indicate that the bus is locked, preventing other devices from accessing it. This is typically used during critical operations where exclusive access to the bus is necessary to ensure data integrity and prevent conflicts.

For more information on each signal, refer to the Motorola MC68030 User Manual.

SE/30 PDS Connnector

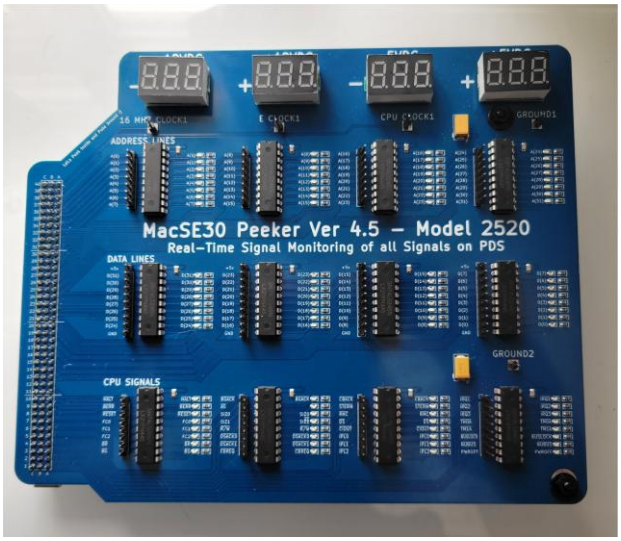


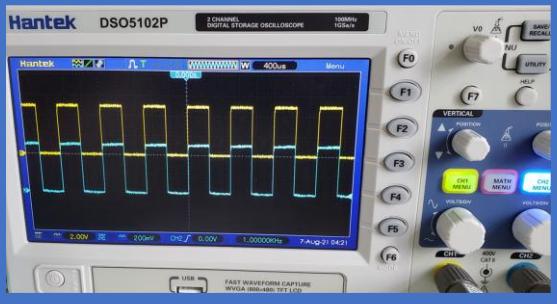
A	B	C	
Reserved	Reserved	PWROFF	1
Reserved	GND	/NUBUS	2
/BUSLOCK	/TM1A	/TM0A	3
/IRQ3	/IRQ2	/IRQ1	4
/IPL2	/IPL1	/IPL0	5
/CIOUT	/DS	/RMC	6
/STERM	/CBACK	/CBREQ_	7
/DSACK1	/DSACK0	R/W	8
SIZ1	SIZ0	/AS	9
/BGACK	/BG	/BR	10
FC2	FC1	FC0	11
/RESET	/BERR	/HALT	12
D0	+5V	D1	13
D2	D3	D4	14
D5	D6	D7	15
D8	GND	D9	16
D10	D11	D12	17
D13	D14	D15	18
D16	+5V	D17	19
D18	D19	D20	20
D21	D22	D23	21
D24	GND	D25	22
D26	D27	D28	23
D29	D30	D31	24
A31	+5V	A30	25
A29	A28	A27	26
A26	A25	A24	27
A23	GND	A22	28
A21	A20	A19	29
A18	A17	A16	30
A15	+5V	A14	31
A13	A12	A11	32
A10	A9	A8	33
A7	GND	A6	34
A5	A4	A3	35
A2	A1	A0	36
+5V	+5V	+5V	37
CPUCLOCK	ECLK	C16M	38
GND	GND	GND	39
-12V	-5V	+12V	40

Macintosh SE/30 PDS Connector Descriptions

Signal name	Signal description
A0-A31	Address bus, bits 0 through 31
FC0-FC2	Function Code
D0-D31	Data bus, bits 0 through 31
/RESET	System reset
/BERR	Bus error
/HALT	Halt
FC0-FC2	Function codes, bits 0 through 2
/BR	Bus request
/BG	Bus grant
/BGACK	Bus grant acknowledge
SIZ0-SIZ1	Transfer size, bits 0 and 1
/AS	Address strobe
/DSACK0 -/DSACK1	Data transfer & size acknowledge, bits 0 & 1
R/W	Read/write
/STERM	Synchronous termination
/CBACK	Cache burst acknowledge
/CBREQ_	Cache burst request
/CIOUT	Cache inhibit out
/DS	Data strobe
/RMC	Read-modify-write cycle
/IPL0 -/IPL2	Interrupt priority lines, bits 0 through 2
CPUCLOCK	16.67 MHz CPU clock
+5V	+5 volts
GND	Ground
PWROFF	Power off
NUBUS	NuBus space access
BUSLOCK	NuBus buslock
/TM0A -/TM1A	NuBus transfer mode, bits 0 & 1
IRQ1-IRQ3	Interrupt inputs
ECLK	E clock
C16M	15.6672MHz gen clock

Rudy’s Retro Intelligence





Apple Macintosh SE/30 Peeker